Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1-5. (Canceled)

6. (Currently amended) A data processing system for profiling an application in the data processing system, the data processing system comprising:

each one of a plurality of individual instructions associated with an indicator that indicates that each one of the plurality of instructions needs to be monitored, the indicator stored in at least one existing spare bit in each one of the plurality of individual instructions;

an instruction cache, which is included in a processor, that outputs said plurality of instructions to a sequencer unit that outputs the plurality of instructions to execution units for executing the plurality of instructions, wherein the sequencer unit and execution units are included in the processor;

the instruction cache for using said indicator to detect execution of each one of the plurality of instructions, wherein execution of instructions, which are not associated with the indicator, is not detected;

~~the instruction cache for detecting execution of a particular one of the plurality of instructions using the indicator that is stored in the at least one existing spare bit in the particular one of the plurality of instructions , wherein the instruction is located in a routine;~~

the instruction cache sending a signal to a performance monitor unit responsive to the instruction cache detecting said indicator in a particular one of the plurality of instructions, wherein the particular one of the plurality of instructions is located in a routine, and further wherein the signal is not sent to the performance monitor unit for instructions that are not associated with the indicator, and further wherein the signal indicates that the particular one of the plurality of instructions is being executed, and still further wherein the performance monitor unit is coupled to each functional unit of said processor;

the performance monitor unit counting events that are associated with an execution of only said plurality of instructions that are associated with the indicator responsive to the performance monitor unit receiving the signal;

collecting means for collecting data from the performance monitor unit;

using means for using said data to identify a caller of the routine;

the instruction cache for determining whether the particular one of the plurality of instructions has been executed more often than a threshold value; and

the instruction cache, responsive to the particular one of the plurality of instructions having been executed more often than the threshold value, for generating an interrupt to pass control to a monitoring program, wherein the monitoring program identifies information regarding the caller of the routine.

7. (Currently amended) The data processing system of claim 6 further comprising:

examining means for examining a call stack upon generation of the interrupt; and

identifying means for identifying the [[a]] caller of the routine from an examination of the call stack.

8. (Currently amended) The data processing system of claim 6, wherein the information includes at least one of the [[a]] caller of the routine and a number of instructions executed in the routine.

9. (Previously Presented) The data processing system of claim 6, further comprising:

generating means for generating a call graph from the information.

10. (Original) The data processing system of claim 6 further comprising:

selecting means for selecting the caller of the routine for analysis based on the information gathered by the monitoring program.

11. (Currently amended) A computer program product~~, which is stored in a computer readable medium,~~ for profiling an application in a data processing system, the computer program product comprising:

a computer-readable medium having stored thereon computer-readable instructions, the computer readable instructions comprising:

[[first]] instructions for associating each one of a plurality of individual instructions with an indicator that indicates that each one of the plurality of instructions needs to be monitored;

~~second~~ instructions for storing said indicator in at least one existing spare bit in each one of the plurality of individual instructions;

said indicator used to detect execution of each one of the plurality of instructions, wherein execution of instructions, which are not associated with the indicator, is not detected;

instructions for outputting, from an instruction cache, the plurality of instructions to a sequencer unit;

instructions for outputting, from the sequencer unit, the plurality of instructions to execution units for executing the plurality of instructions, wherein the sequencer unit and execution units are included in the processor;

instructions for sending, by the instruction cache, a signal to a performance monitor unit responsive to the instruction cache detecting said indicator in a particular one of the plurality of instructions, wherein the particular one of the plurality of instructions is located in a routine, and further wherein the signal is not sent to the performance monitor unit for instructions that are not associated with the indicator, and further wherein the signal indicates that the particular one of the plurality of instructions is being executed, and still further wherein the performance monitor unit is coupled to each functional unit of said processor;

instructions for counting, by the performance monitor unit, events that are associated with an execution of only said plurality of instructions that are associated with the indicator responsive to the performance monitor unit receiving the signal;

instructions for collecting data from the performance monitor unit;

instructions for using said data to identify a caller of the routine;

~~third instructions for detecting, by an instruction cache, execution of a particular one of the plurality of instructions using the indicator that is stored in the at least one existing spare bit in the particular one of the plurality of instructions , wherein the instruction is located in a routine;~~

~~fourth~~ instructions for determining, by the instruction cache, whether the particular one of the plurality of instructions has been executed more often than a threshold value; and

[[fifth]] instructions, responsive to the particular one of the plurality of instructions having been executed more often than the threshold value, for generating, by the instruction cache, an interrupt to pass control to a monitoring program, wherein the monitoring program identifies information regarding the caller of the [[a]] routine.

12. (Currently amended) The computer program product of claim 11 further comprising:

[[sixth]] instructions for examining a call stack upon generation of the interrupt; and

~~seventh~~ instructions for identifying the [[a]] caller of the routine from an examination of the call stack.

13. (Currently amended) The computer program product of claim 11, wherein the information includes at least one of the [[a]] caller of the routine and a number of instructions executed in the routine.

14. (Currently amended) The computer program product of claim 11 further comprising:

[[sixth]] instructions for generating a call graph from the information.

15. (Currently amended) The computer program product of claim 11 further comprising:

[[sixth]] instructions for selecting the caller of the routine for analysis based on the information gathered by the monitoring program.

16. (Currently amended) The data processing system according to claim 6, further comprising:

the indicator stored in a plurality of existing spare bits in each one of the plurality of instructions;

a first one of the plurality of bits indicating that each execution of each one of the plurality of instructions should be counted;

a second plurality [[one]] of the plurality of bits identifying the threshold value; and

a third plurality [[one]] of the plurality of bits used as a counter to count a number of times each one of the plurality of instructions is executed.

17. (Previously Presented) The data processing system according to claim 16, further comprising:

a set of registers for controlling a meaning of each one of the plurality of bits.

18. (Currently amended) The computer program product according to claim 11, further comprising:

the second instructions for storing the indicator in a plurality of existing spare bits in each one of the plurality of instructions;

a first one of the plurality of bits indicating that each execution of each one of the plurality of instructions should be counted;

a second plurality [[one]] of the plurality of bits identifying the threshold value; and

a third plurality [[one]] of the plurality of bits used as a counter to count a number of times each one of the plurality of instructions is executed.

19. (Currently amended) A computer program product~~, which is stored in a computer readable medium,~~ for profiling an application in a data processing system, the computer program product comprising:

a computer-readable medium having stored thereon computer-readable instructions, the computer readable instructions comprising:

[[first]] instructions for associating each one of a plurality of individual instructions with an indicator that indicates that each one of the plurality of individual instructions needs to be monitored;

~~second~~ instructions for storing the indicator in a plurality of existing spare bits in each one of the plurality of individual instructions;

said indicator used to detect execution of each one of the plurality of instructions, wherein execution of instructions, which are not associated with the indicator, is not detected;

instructions for outputting, from an instruction cache, the plurality of instructions to a sequencer unit;

instructions for outputting, from the sequencer unit, the plurality of instructions to execution units for executing the plurality of instructions, wherein the sequencer unit and execution units are included in the processor;

instructions for sending, by the instruction cache, a signal to a performance monitor unit responsive to the instruction cache detecting said indicator in a particular one of the plurality of instructions, wherein the particular one of the plurality of instructions is located in a routine, and further wherein the signal is not sent to the performance monitor unit for instructions that are not associated with the indicator, and further wherein the signal indicates that the particular one of the plurality of instructions is being executed, and still further wherein the performance monitor unit is coupled to each functional unit of said processor;

instructions for counting, by the performance monitor unit, events that are associated with execution of only said plurality of instructions that are associated with the indicator responsive to the performance monitor unit receiving the signal;

instructions for collecting data from the performance monitor unit;

instructions for using said data to identify a caller of the routine;

~~third instructions for detecting, by an instruction cache, execution of a particular one of the plurality of instructions using the indicator that is stored in the plurality of existing spare bits in the particular one of the plurality of instructions, wherein the particular one of the plurality of instructions is located in a routine;~~

~~fourth instructions for sending, by the instruction cache, a signal to a performance monitor unit in response to detecting execution of said particular one of the plurality of instructions;~~

[[fifth]] instructions for determining, by the instruction cache, whether the particular one of the plurality of instructions has been executed more often than a threshold value, the threshold value being a number of clock cycles that are needed to complete the particular one of the plurality of instructions;

[[sixth]] instructions responsive to the particular one of the plurality of instructions having been executed more often than the threshold value: for generating, by the instruction cache, an interrupt to pass control to a monitoring program, wherein the monitoring program identifies information regarding the [[a]] caller of the routine.

~~seventh~~ instructions for examining a call stack upon generation of the interrupt;

~~eighth~~ instructions for identifying a caller of the routine from an examination of the call stack;

wherein the information includes the caller of the routine and a number of instructions executed in the routine;

instructions for generating a call graph from the information;

instructions for selecting the caller of the routine for analysis based on the information gathered by the monitoring program;

a first one of the plurality of bits indicating that each execution of each one of the plurality of instructions should be counted;

a second plurality [[one]] of the plurality of bits identifying the threshold value;

a third plurality [[one]] of the plurality of bits used as a counter to count a number of times each one of the plurality of instructions is executed; and

instructions for controlling, by a set of registers, a meaning of each one of the plurality of bits.